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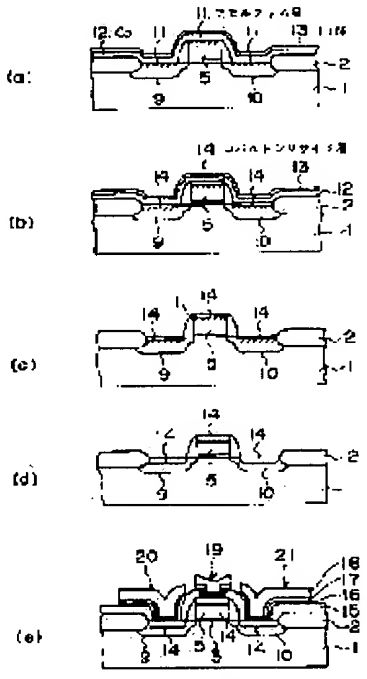
(54) MANUFACTURING METHOD FOR SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To form a cobalt silicide layer wherein a spike is hard to occur on the bottom surface, relating to a manufacturing method for a semiconductor device containing a salicide process.
SOLUTION: On the upper layer part of an impurity diffusion layer 9 of a silicon, an amorphous layer 11 is formed by ion implantation, and after an cobalt film 12 is formed on the impurity diffusion layer 9, the cobalt film 12 and the silicon in the impurity diffusion layer 9 are made to react each other in the first thermal treatment, so that a cobalt silicide layer 14 made of CoSi or Co2Si at low temperature is formed on the upper layer part of the amorphous layer 11. Then, no-reaction cobalt is removed, and in the second thermal treatment, the CoSi or Co2Si constituting the cobalt silicide layer 14 is decomposed into CoSi2 for lower resistance, and at the same time, the cobalt silicide layer 14 is made protruded up to the depth of the initial amorphous layer 11 or further.



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[Claim(s)]

[Claim 1] The manufacture method of a semiconductor device characterized by providing the following. The process which introduces an impurity into the management of a silicon layer and forms an impurity diffusion layer with heat treatment The process which forms an amorphous layer in the management of the aforementioned impurity diffusion layer by carrying out the ion implantation of the element The process which forms a cobalt film on the aforementioned amorphous layer The aforementioned cobalt film and the aforementioned impurity diffusion layer are heated with the 1st temperature, and it is Co2Si to the management of the aforementioned amorphous layer. Or the process which forms the cobalt silicide layer which consists of CoSi, The silicon in the aforementioned impurity diffusion layer, the process which removes the aforementioned cobalt film which did not react, and by heating the aforementioned cobalt silicide layer and the aforementioned impurity diffusion layer with the 2nd temperature the aforementioned Co2Si or CoSi -- CoSi2 Process which forms the aforementioned cobalt silicide layer more deeply than the same depth as the aforementioned amorphous layer, or the aforementioned amorphous layer while making it change

[Claim 2] The 1st temperature of the above is the manufacture method of the semiconductor device according to claim 1 characterized by being 450 degrees C or less.

[Claim 3] The 2nd temperature of the above is the manufacture method of the semiconductor device according to claim 1 characterized by being lower than the temperature in the case of the aforementioned heat treatment which is 500 degrees C or more and forms an impurity diffusion layer.

[Claim 4] The aforementioned cobalt film is the manufacture method of the semiconductor device according to claim 1 characterized by forming in the thickness of 8-20nm.

[Claim 5] The manufacture method of the semiconductor device according to claim 1 characterized by forming a cap layer on the aforementioned cobalt film before performing the aforementioned heat treatment after forming the aforementioned cobalt film.

[Claim 6] The aforementioned element is the manufacture method of the semiconductor device according to claim 1 characterized by being germanium, silicon, and arsenic.

[Claim 7] The aforementioned germanium is 8x1013 atoms/cm2. An ion implantation is carried out above, the ion implantation of the aforementioned silicon is carried out by two or more 8x1014 atoms/cm, and the aforementioned arsenic is 8x1013 atoms/cm2 - 5x1014 atoms/cm2. The manufacture method of the semiconductor device according to claim 6 characterized by carrying out an ion implantation.

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] this invention relates to the manufacture method of a semiconductor device of having a salicide process, in more detail about the manufacture method of a semiconductor device.

[0002]

[Description of the Prior Art] High integration of today's semiconductor device and speed-izing of high-speed-izing can be remarkable, and can enjoy now easily high speed the image processing of 3-dimensional one, high-speed communication, etc. with a domestic personal computer and a domestic game machine. Such highly efficient-ization has been realized by only making size of a CMOS device detailed. The present CMOS

device is in the mass-production stage of a size where gate length is about 0.35 micrometers, and the 0.1 -0.O5micrometer CMOS device is also reported by research level. However, the parasitism resistance according to a scaling law becomes large, and a performance does not go up as the conventional trend by the device by which gate length becomes smaller than 0.35 micrometers. Then, the process which silicide-izes the gate, the source, and a drain simultaneously, and forms them into low resistance, i.e., a salicide process, is indispensable technology.

[0003] In the MOS transistor, if a diffusion layer is made shallow in order to stop the short channel effect etc., since increase of resistance of a diffusion layer will be brought about, the technology which silicide-izes the polysilicon contest front face which constitutes a gate electrode, and the front face of a source layer and a drain layer on a self-adjustment target, and forms them into low resistance on him is examined. As the silicide, material, such as TiSi2, CoSi2, and NiSi, is used.

[0004] Next, the general manufacturing process of the MOS transistor which used Co Salicide for the surface of the gate, the source, and a drain is explained. First, drawing 20 (a) It is the silicon machine hill 101 so that it may be shown. It is LOCOS inside. Oxide film 102 It is the about 50A gate oxide film 103 by thermal oxidation about the front face of the separated field. It forms. Then, it is the polysilicon contest film 104 of about 1500A thickness by CVD on it. It forms.

[0005] Next, drawing 20 (b) It is the polysilicon contest film 104 so that it may be shown. After carrying out the ion implantation of either PORON, Lynn or arsenic inside, it is the polysilicon contest film 104. Patterning is carried out and it is the gate electrode 105. It forms. The ion implantation of the next door is carried out next, and it is the shallow impurity pouring layer 106. It forms. next, drawing 20 (c) it is shown -- as -- CVD -- a silicon oxide with a thickness of about 1000A -- forming -- gate electrode 105 until it exposes -- anisotropic etching -- carrying out -- a silicon oxide -- sidewall 107 ****** -- it leaves

[0006] After that, the ion implantation of the next door is carried out, and it is the deep impurity pouring layer 108. Impurity pouring layer 106 shallow after forming Deep impurity pouring layer 108 It is activated by heat-treatment and, thereby, is the gate electrode 105. Silicon substrate 101 of both sides Source layer 109 of LDD structure Drain layer 110 It will form. next, buffered fluoric acid -- the gate electrode 105, the source layer 109, and drain layer 110 after removing the silicon oxide (natural oxidation film) of each front face -- drawing 20 (d) it is shown -- as -- About 100A cobalt film 111 About 300A titanium-nitride film 112 forming -- RTA for 550 ** 30 seconds (rapid thermal annealling) processing -- silicide ---izing -- cobalt silicide layer 113 It forms.

[0007] Then, drawing 20 (e) It is the titanium-nitride film 112 so that it may be shown. The unreacted cobalt film 111 is removed and it is RTA for further 850 **30 seconds. It processes and, thereby, they are the gate electrode 105 and the source layer 109. And drain layer 110 The cobalt silicide layer 114 formed in the front face is further formed into low resistance. Such Salicide technology is a fundamental process, as the improvement technology, the flattening technology of a silicide layer is shown in JP,62-33466,A, and the equalization technology of the thickness of a silicide layer is indicated by JP,5-291180,A.

[0008]

[Problem(s) to be Solved by the Invention] Although there is especially no problem when

formation of the above cobalt silicide layers has a source layer and a deep drain layer, when it becomes shallow, for example to about 100nm, there is a problem that a leakage current becomes easy to flow. It thinks for the spike of cobalt silicide occurring from the bottom of a cobalt silicide layer, and running through a source layer and a drain layer as the cause. The spike of such cobalt silicide was produced even if formed according to the method and temperature conditions which were indicated by two patent official reports which described the cobalt silicide layer above.

[0009] this invention is made in view of such a problem, and aims at offering the manufacture method of a semiconductor device including the process which forms the cobalt silicide layer which a spike cannot produce easily on a base.

[0010]

[Means for Solving the Problem]

The process which introduces an impurity into the management of the silicon layer 1, and forms the impurity diffusion layers 9 and 10 with heat treatment so that the above-mentioned technical problem may be illustrated to drawing 1 and 2, (Means) The process which forms the amorphous layer 11 in the management of the aforementioned impurity diffusion layers 9 and 10 by carrying out the ion implantation of the element, The process which forms the cobalt film 12 on the aforementioned amorphous layer 11, and the aforementioned cobalt film 12 and the aforementioned impurity diffusion layers 9 and 10 are heated with the 1st temperature. The process which forms in the management of the aforementioned amorphous layer 11 the cobalt silicide layer 14 which consists of Co2 Si or CoSi, The aforementioned impurity diffusion layer 9, the silicon in ten and the process which removes the aforementioned cobalt film 12 which did not react, and by heating the aforementioned cobalt silicide layer 14 and the aforementioned impurity diffusion layers 9 and 10 with the 2nd temperature the aforementioned Co2Si or CoSi -- CoSi2 While making it change, it solves by the manufacture method of the semiconductor device characterized by having the process which forms the aforementioned cobalt silicide layer 14 more deeply than the same depth as the aforementioned amorphous layer 11, or the aforementioned amorphous layer 11.

[0011] In the manufacture method of the above-mentioned semiconductor device, it is characterized by the 1st temperature of the above being 450 degrees C or less. In the manufacture method of the above-mentioned semiconductor device, the 2nd temperature of the above is characterized by being lower than the temperature in the case of the aforementioned heat treatment which is 500 degrees C or more and forms an impurity diffusion layer. In the manufacture method of the above-mentioned semiconductor device, it is characterized by forming the aforementioned cobalt film in the thickness of 8-20nm.

[0012] In the manufacture method of the above-mentioned semiconductor device, after forming the aforementioned cobalt film, before performing the aforementioned heat treatment, it is characterized by having the process which forms cobalt and the cap layer (for example, TiN) which does not react on the aforementioned cobalt film. In the manufacture method of the above-mentioned semiconductor device, the aforementioned element is characterized by being germanium, silicon, and arsenic. In this case, the aforementioned germanium is 8x1013 atoms/cm2. An ion implantation is carried out above, the ion implantation of the aforementioned silicon is carried out by two or more 8x1014 atoms/cm, and the aforementioned arsenic is 8x1013 atoms/cm2 - 5x1014 atoms/cm2. It is

characterized by carrying out an ion implantation.

[0013] (Operation) Next, an operation of this invention is explained. In order to form a cobalt silicide layer in the management of an impurity diffusion layer according to this invention An amorphous layer is formed in the management of the impurity diffusion layer which consists of silicon with an ion implantation. After forming a cobalt film on an impurity diffusion layer furthermore, a cobalt film and the silicon in an impurity diffusion layer are made to react with the 1st heat treatment, and they are CoSi or Co2Si at low temperature to the management of the amorphous layer. The becoming cobalt silicide layer is formed. Then, CoSi or Co2Si which removes an unreacted cobalt film and subsequently constitutes a cobalt silicide layer with the 2nd heat treatment CoSi2 While making it change and forming sheet resistance into low resistance It is the same as the depth of an early amorphous layer, or the cobalt silicide layer is made to enter more deeply than it.

[0014] According to such a process, movement in the lower part of the composition element of a cobalt silicide layer is barred by the amorphous layer in the case of the 1st heat treatment for forming a cobalt silicide layer, and the 2nd heat treatment, and generating of a spike of a cobalt silicide layer is prevented. And since it was made for the recrystallization to make it immersed by the cobalt silicide layer even if it extended the cobalt silicide layer to the depth in early stages of an amorphous layer and the amorphous layer recrystallized on the occasion of the 2nd heat treatment, junction in the high recrystallization of resistance and a cobalt silicide layer is barred, and elevation of contact resistance is prevented.

[0015] If the temperature of the 1st heat treatment becomes 450 degrees C or more, since an amorphous layer will carry out lower shell recrystallization, the meaning made amorphous is lost. Moreover, if it is more than the temperature for the temperature of the 2nd heat treatment activating an impurity diffusion layer, since cobalt will begin to melt from a silicide layer and junction leak will be increased, it is not desirable. Such a cobalt silicide layer is used for the source layer of an MOS transistor, a drain layer, etc., and forms those layers into low resistance.

[0016] In addition, although especially the element that carries out an ion implantation in order to form an amorphous layer is not limited, germanium with big mass, silicon, its arsenic used for a dopant are desirable.

[0017]

[Embodiments of the Invention] Then, the operation gestalt of this invention is explained based on a drawing below. Below, the gestalt of operation of this invention is explained. Drawing 1 is the cross section showing the process of 1 operation gestalt of this invention. First, drawing 1 (a) It is LOCOS among the silicon machine hills 1 so that it may be shown. The front face of the field separated by the oxide film 2 is oxidized thermally, and it is 5nm in thickness by this. The gate oxide film 3 of a grade is formed. Then, the gate oxide film 3 and LOCOS It is 150nm by CVD on an oxide film 2. The polysilicon contest film 4 of the thickness of a grade is formed.

[0018] Next, drawing 1 (b) After carrying out the ion implantation of the arsenic into the polysilicon contest film 4 so that it may be shown, patterning of the polysilicon contest film 4 and the gate oxide film 3 is carried out, and the gate electrode 5 is formed with the polysilicon contest film 4. The ion implantation of the arsenic is carried out to a mask at a silicon substrate 1, using the gate electrode 5, and the shallow impurity pouring layer 6 is formed next. the dose of the ion implantation -- 3x1014 atm/cm2 it is -- the acceleration

energy -- 10keV(s) it is .

[0019] Next, it is 100nm by CVD. The silicon oxide of the thickness of a grade is formed. Then, anisotropic etching of the silicon oxide is perpendicularly carried out until the upper surface of the gate electrode 5 is exposed, and it is drawing 1 (c). It leaves a silicon oxide to the side of the gate electrode 5 as a sidewall 7 so that it may be shown. After that, the ion implantation of the arsenic is carried out to a mask at a silicon substrate 1 using the gate electrode 5, and the deep impurity pouring layer 8 is formed. the dose of the ion implantation -- 2x1015 atm/cm2 it is -- the acceleration energy -- 40keV(s) it is .

[0020] Next, while making the interior diffuse the arsenic in the gate electrode 5 by RTA processing for 10 seconds at 1000 degrees C, the arsenic of the shallow impurity pouring layer 6 and the deep impurity pouring layer 8 is activated, and it is drawing 1 (d). The source layer 9 and the drain layer 10 of LDD structure as shown are formed in the silicon substrate 1 of the both sides of the gate electrode 5. In this case, the depth of the field which does not lap with a sidewall 7 among the source layer 9 and the drain layer 10 is set to about 100nm from the front face of a silicon substrate 1.

[0021] After that, it is drawing 1 (e). The ion implantation of the germanium is carried out to the whole containing the source layer 9 and the drain layer 10, and this forms the amorphous (amorphous) layer 11 in the surface of the gate electrode 5, the source layer 9, and the drain layer 10 so that it may be shown. The ion implantation is dose 8x1013 atm/cm2. It is above. Moreover, the amorphous layer 11 is formed more shallowly than the bottom of the source layer 9 and the drain layer 10, and the acceleration energy at the time of an ion implantation is deep to the grade to which the amorphous layer 11 moreover does not disappear at the time of the 1st next heat-treatment for silicide-izing, and is set as the size in which the amorphous layer 11 disappears further at the time of the 2nd heat-treatment for silicide-izing.

[0022] Although specifically based on the depth of the silicide layer which it is going to form from now on, when the depth of the source layer 9 and the drain layer 10 is 100nm, it is 20-40keV. It is within the limits of a grade. then, buffered fluoric acid -- the gate electrode 5, the source layer 9, and the drain layer 10 -- the silicon oxide of each front face is removed Buffered fluoric acid is the mixed liquor of the rate of 100 about 2 and water in fluoric acid, and the removal time is about 60 seconds.

[0023] Next, drawing 2 (a) The cobalt (Co) film 12 with a thickness of about 8-20nm and the about 30nm titanium-nitride (TiN) film 13 are formed in the whole one by one by the spatter so that it may be shown. On the occasion of growth of the cobalt film 12, the amount of direct current powers which impresses the argon quantity of gas flow to 5mTorr(s) and growth atmosphere to 100sccm(s) and a cobalt target for the growth ambient-pressure force was made into 0.2 W/cm2. Thickness of the cobalt film 12 is made so thick that germanium ion-implantation energy is enlarged.

[0024] Moreover, on the occasion of growth of the titanium-nitride film 13, the amount of direct current powers which impresses the argon quantity of gas flow to 5mTorr(s) and growth atmosphere to 50sccm(s), and impresses a nitrogen gas flow rate to 50sccm(s) and a titanium-nitride target for the growth ambient-pressure force was made into 7.0 W/cm2. The titanium-nitride film 13 is formed in order to suppress that irregularity arises on the front face of a silicide layer in the case of silicide-izing.

[0025] After that, the 1st above-mentioned heat-treatment for silicide-izing is performed.

That is, if RTA (rapid thermal annealling) processing for 30 seconds is performed at 400-450 degrees C and each front face of the gate electrode 5, the source layer 9, and the drain layer 10 is silicide-ized in the atmosphere of nitrogen or an argon as shown in drawing 2 (b), it is Co2Si to the upper part of the amorphous layer 11. Or the cobalt silicide layer 14 which consists of CoSi is formed. In addition, since it recrystallizes the bottom of the amorphous layer 11 when the cobalt silicide layer 14 will not be formed if RTA temperature becomes lower than 400 degrees C, and it becomes higher than 450 degrees C, it is not desirable. Since the ion-implantation energy of germanium is optimized as described above, the amorphous layer 11 did not disappear in this stage, and although the upper part of the amorphous layer 11 not only corrodes by the cobalt silicide layer 14, but single-crystal-izes from a bottom among the amorphous layers 11 at the time of this heat-treatment, even when it is small, it remains.

[0026] Next, drawing 2 (c) Mixed liquor of the hydrogen peroxide heated at 70 degrees C so that it might be shown, and aqueous ammonia (H2O2:NH4 OH:H2O =1:1:4) By soaking for 180 seconds, the titanium-nitride film 13 is removed and continued and it is the mixed liquor (H2SO4:H2O2 =3:1) of a sulfuric acid and a hydrogen peroxide. The unreacted cobalt film 12 is removed by soaking for 20 minutes. In this case, the cobalt silicide layer 14 remains as it is.

[0027] Next, 2nd heat-treatment for silicide-izing is performed. Namely, drawing 2 (d) The cobalt silicide layer 14 is heated by the 600 degrees C - 900 degrees C temperature requirement in the atmosphere of nitrogen or an argon so that it may be shown. Thereby, the cobalt silicide layer 14 is Co2Si. Or CoSi to CoSi2 Low resistance is changed and formed. In this case, it is CoSi2 when heating temperature is made lower than 600 degrees C. It is hard coming to be generated and it becomes impossible to attain low resistance-ization. Moreover, if heating temperature becomes high from 900 degrees C or more, Co atom will begin to melt from the cobalt silicide layer 14, and junction leak will be increased.

[0028] The thickness of the cobalt silicide layer 14 obtained by this is 0.5-2.0, when thickness in which the impurity diffusion layer which constitutes the source layer 9 and the drain layer 10 remained is set to 1. It becomes a grade. To next, it is drawing 2 (e). The silicon oxide 15 with a thickness of 700nm is formed in the whole by CVD so that it may be shown. subsequently After carrying out patterning of the silicon oxide 15 and forming a contact hole on the gate electrode 5, the source layer 9, and the drain layer 10 The titanium film 16 of 20nm of thickness, the titanium-nitride film 17 of 100nm of thickness, and the aluminum layer 18 of 500nm of thickness are formed. Patterning of these three layers 16-18 is carried out by the photo lithography method, and the general gate drawer electrode 19, the source drawer electrode 20, and the drain drawer electrode 21 are formed.

[0029] In addition, although germanium was used in the above-mentioned explanation in order to form the amorphous layer 14, you may carry out the ion implantation of other elements, such as silicon, arsenic, and boron. In addition, germanium and silicon are desirable when the mass of an element, control of the high impurity concentration of an impurity diffusion layer, etc. are taken into consideration. The ion implantation of the germanium is carried out by two or more 8x1013 atoms/cm, the ion implantation of the silicon is carried out by two or more 8x1014 atoms/cm, and the ion implantation of the arsenic is carried out by 8x1013 atoms/cm2 - 5x1014 atoms/cm2.

[0030] At the pars basilaris ossis occipitalis of the cobalt silicide layer 14 in the MOS

transistor formed of the above processes, a spike hardly occurred, but the leakage current was suppressed. Below, spike generating of the cobalt silicide layer 14 is explained in full detail. Drawing 3 (a) After forming the cobalt layer 12 of 10nm of thickness on it without changing a silicon substrate 1 amorphously so that it may be shown, the 1st experiment as shown below was conducted.

[0031] First, drawing 3 (b) It is Co2Si when the cobalt layer 12 and the silicon substrate 1 were heated at 400 degrees C so that it might be shown. The cobalt silicide layer 14 shown was formed in the surface of a silicon substrate 1. Next, drawing 3 (c) Co2Si which constituted the cobalt silicide layer 14 when the cobalt silicide layer 14 and the silicon substrate 1 were heated at 450 degrees C so that it might be shown It changed to CoSi. Then, drawing 3 (d) CoSi is CoSi2 when the cobalt silicide layer 14 was heated at 600 more degrees C so that it might be shown. It changed and, moreover, the spike 22 had arisen in the base of the cobalt silicide layer 14. CoSi2 after removing unreacted cobalt When transverse-electromagnetic observation of the cross section of the interface of Si was carried out, it came to be shown in drawing 4 , and the interface is irregular and unusual growth (spike) of the shape of about 80nm icicle had produced it at the maximum.

[0032] Next, drawing 5 (a) After turning a silicon substrate 1 amorphously shallowly from a front face so that it may be shown, the cobalt layer 12 of 10nm of thickness was formed on it, and the 2nd experiment as subsequently to a degree shown was conducted. First, drawing 5 (b) It is Co2Si when the cobalt layer 12 and the silicon substrate 1 were heated at 400 degrees C so that it might be shown. The cobalt silicide layer 14 shown was formed in silicon-substrate 1 surface, and the thin amorphous layer 11 remained in the pars basilaris ossis occipitalis. Next, it is drawing 5 (c). Co2Si which constitutes the cobalt silicide layer 14 when the cobalt layer 14 and silicon substrate 1 which were heated at 400 degrees C are heated at 450 more degrees C so that it may be shown It changed to CoSi and, moreover, the cobalt silicide layer 14 corroded the amorphous layer 11 altogether. And the spike had arisen in the base of the cobalt silicide layer 14. Furthermore, drawing 5 (d) It is CoSi2 when the cobalt silicide layer 14 was again heated at 600 degrees C so that it might be shown. The cobalt silicide layer 14 shown was formed and the spike 22 had arisen in the base.

[0033] Next, drawing 6 (a) After turning the surface of a silicon substrate 1 amorphously deeply so that it may be shown, the cobalt layer 12 of 10nm of thickness was generated, and the 3rd experiment shown further below was conducted. First, drawing 6 (b) It is Co2Si when the cobalt layer 12 and the silicon substrate 1 were heated at 400 degrees C so that it might be shown. The cobalt silicide layer 14 shown was formed in the surface of a silicon substrate 1, and the thick amorphous layer 11 remained in the pars basilaris ossis occipitalis. Then, drawing 6 (c) Co2Si which constitutes the cobalt silicide layer 14 when the cobalt silicide layer 14 and silicon substrate 1 which were heated at 400 degrees C are heated at 450 more degrees C so that it may be shown Although it changed to CoSi and the amorphous layer 11 existed in the lower part, the pars basilaris ossis occipitalis of the amorphous layer 11 was recrystallized slightly. Furthermore, drawing 6 (d) It is CoSi2 when the cobalt silicide layer 14 was again heated at 600 degrees C so that it might be shown. The cobalt silicide layer 14 shown was formed, and spike 22 did not arise in the base, but, moreover, the silicon layer 23 of the result which the amorphous layer 11 recrystallized existed in the lower part.

[0034] Therefore, in order to prevent generating of the spike from the cobalt silicide layer 14, it is thought that what is necessary is just to make the amorphous layer 11 deep enough like the process of the 3rd experiment. As shown in drawing 2 in fact, a source layer and a drain layer exist in the silicon layer 23 which recrystallized, and the heating temperature of about 850 degrees C is not enough as activation of the impurity in the amorphous layer 11, and it becomes impossible however, for contact resistance with the cobalt silicide layer 14, and a source layer / drain layer to fully reduce it. Thereby, the original purpose of silicide-izing called the reduction in resistance of a source layer and a drain layer cannot be attained.

[0035] Next, drawing 7 (a) After turning the surface of a silicon substrate amorphously so that it may be shown, the cobalt layer 12 of 10nm of thickness was formed, and the 4th experiment shown below was conducted further. That is [it made the depth of the amorphous layer 11 into the proper value], it was made for the cobalt silicide layer 14 to also corrode the silicon layer 23 which the amorphous layer 11 existed under the cobalt silicide layer 14 after the 1st heat-treatment, and was recrystallized of the amorphous layers 11 in the reheating processing which is 600 degrees C in this experiment.

[0036] First, drawing 7 (b) It is Co2Si when the cobalt layer 12 and the silicon substrate 1 were heated for 30 seconds at 400 degrees C so that it might be shown. The cobalt silicide layer 14 shown was formed in silicon-substrate 1 surface, and the amorphous layer 11 remained in the lower part. Then, drawing 7 (c) Co2Si which constitutes the cobalt silicide layer 14 when the cobalt silicide layer 14 and a silicon substrate 1 are heated for 30 seconds at 450 more degrees C so that it may be shown It changed to CoSi. Moreover, thickness is 20.2nm and the cobalt silicide layer 14 changed into the state where 2.0mm projected from the front face of a silicon substrate 1, among those. Moreover, the silicon layer 23 and the amorphous layer 11 which were recrystallized under the cobalt silicide layer 14 existed, and such thickness was 18.2nm or less in total.

[0037] Furthermore, drawing 7 (d) CoSi which constituted the cobalt silicide layer 14 when the cobalt silicide layer 14 and the silicon substrate 1 were reheated for 30 seconds at 600 degrees C so that it might be shown is CoSi2. It became and was thick thin with 35.2nm. In this case, since 1.2nm of cobalt silicide layers 14 sank and they existed from the front face of a silicon substrate 1, the amorphous layer 14 of the beginning was completely corroded in the cobalt silicide layer 14, and, moreover, the silicon layer 23 which recrystallized did not exist in the lower part.

[0038] Therefore, the state of low resistance where the source layer and drain layer which exist under the cobalt silicide layer 14 were first activated at about 1000 degrees C has been maintained, and, thereby, contact resistance with the cobalt silicide layer 14, and a source layer and a drain layer was good. Moreover, CoSi2 When transverse-electromagnetic observation of the interface of Si was carried out, unusual growth like drawing 4 was not seen, but the interface was comparatively flat.

[0039] From the above thing, the cobalt film of 10nm - 20nm of thickness is formed. this by the 1st time The temperature of 400 degrees C - 450 degrees C, It heats for 30 seconds at the temperature of 600-900 degrees C by the 2nd time, respectively, and is CoSi2. In forming the cobalt silicide layer 14 It turns out that it is necessary to form the amorphous layer 11 so that it may become about 18.2nm - 26.4nm or more a depth of 35.2nm - 70.2nm or less to each thickness.

[0040] Moreover, Co2Si Or it is effective if it carries out on the temperature conditions which a silicide reaction occurs and make recrystallization speed of the amorphous layer 11 extremely late in forming the silicide layer 14 which consists of CoSi. For example, as shown in drawing 8 , the recrystallization speed of the amorphous layer 11 becomes extremely slow below 450 degrees C. Moreover, when forming the amorphous layer 11, it turns out that the direction in the case of containing an impurity has a recrystallization speed slower than the case where an impurity is not contained.

[0041] Finally, the leakage current of a cobalt silicide layer is explained. As shown in drawing 9 , while the leakage current grounded the silicon substrate 31, it impressed positive voltage to the cobalt silicide layer 33 of the management of the impurity diffusion layer 32. First, the case where the ion implantation of the germanium is not carried out is explained. Immediately after [forming the cobalt silicide layer 33 and removing unreacted cobalt after that by 550 degrees C and 1st RTA for 30 seconds,], Namely, the relation of the leakage current and bias voltage just behind a washout The place which changed and investigated the plane area of the impurity diffusion layer 32 about (it is hereafter called a leakage-current property), Drawing 10 (a) - (c) When the result as shown was obtained and the circumference length of the impurity diffusion layer 32 was changed and investigated about the leakage-current property, it is drawing 11 (a). - (c) The result as shown was obtained.

[0042] Furthermore, it is CoSi2 by 825 degrees C and 2nd RTA for 30 seconds. The place which changed and investigated the area of the impurity diffusion layer 32 about the leakage-current property after forming the becoming cobalt silicide layer 33, drawing 12 (a) - (c) the place which the result as shown was obtained, and changed and investigated the circumference length of the impurity diffusion layer 32 about the leakage-current property -- drawing 13 (a) and (b) The result as shown was obtained.

[0043] According to drawing 10 - drawing 13 , the leakage-current property after 1st RTA has deteriorated, so that it is bad and circumference length becomes [the area of the impurity diffusion layer 32] larger than the leakage-current property of 2nd RTA for a long time. This is based on the spike of the pars basilaris ossis occipitalis of the cobalt silicide layer 33. Next, the case where poured in germanium and the management of the impurity diffusion layer 32 is turned amorphously beforehand is explained.

[0044] When the plane area of the impurity diffusion layer 32 was changed and investigated about the leakage-current property just behind a washout through 550 degrees C and 1st RTA for 30 seconds, it is drawing 14 (a). - (c) When the result as shown was obtained and the circumference length of the impurity diffusion layer 32 was changed and investigated about the leakage-current property, it is drawing 15 (a). - (c) The result as shown was obtained.

[0045] Furthermore, it is CoSi2 by 825 degrees C and 2nd RTA for 30 seconds. The place which changed and investigated the area of the impurity diffusion layer 32 about the leakage-current property after forming the becoming cobalt silicide layer 33, drawing 16 (a) - (c) the place which the result as shown was obtained, and changed and investigated the circumference length of the impurity diffusion layer 32 about the leakage-current property -- drawing 17 (a) and (b) The result as shown was obtained.

[0046] According to drawing 14 - drawing 17 , when it turns amorphously with the ion implantation of germanium, there is little variation in a leakage-current property, and,

moreover, most of the area of the impurity diffusion layer 32 and the dependency of circumference length is not seen. Next, the result investigated about the cobalt thickness dependency of the leakage-current property of the cobalt silicide layer 33 after 2nd RTA is shown in drawing 18 and drawing 19 .

[0047] When the case where an ion implantation was carried out to the case where the ion implantation of the germanium is not carried out when a cobalt film is 10nm was compared from drawing 18 and 19 and a cobalt film is thickened with 18nm although a difference was hardly seen about a leakage-current property among them, it turns out that a clearly good leakage-current property is acquired for the direction at the time of carrying out the ion implantation of the germanium.

[0048] In addition, although sheet resistance of the cobalt silicide layer at the time of forming a cobalt silicide layer, having used thickness of a cobalt film as 18nm was investigated, they were about 4ohm/** irrespective of the existence of a germanium ion implantation. Before forming a cobalt film, when the ion implantation of the germanium is carried out and it is made amorphous to a silicon substrate also by the above experimental result, it turns out that the few good junction property of the area dependency of an impurity diffusion layer, a circumference length dependency, and a cobalt thickness dependency is acquired.

[0049]

[Effect of the Invention] In order [which was described above] to form a cobalt silicide layer in the management of an impurity diffusion layer like according to this invention After forming an amorphous layer in the management of the impurity diffusion layer which consists of silicon with an ion implantation After forming a cobalt film on an impurity diffusion layer, a cobalt film and the silicon in an impurity diffusion layer are made to react with the 1st heat treatment, and they are CoSi or Co2Si at low temperature to the management of the amorphous layer. Form the becoming cobalt silicide layer, and an unreacted cobalt film is removed continuously. Subsequently, CoSi or Co2Si which constitutes a cobalt silicide layer with the 2nd heat treatment CoSi2 While making it change and forming low resistance By **'s which is the same as an early amorphous layer, or is made to enter more deeply than it, a cobalt silicide layer In the case of the 1st heat treatment for forming a cobalt silicide layer, and the 2nd heat treatment, movement in the lower part of the composition element of a cobalt silicide layer is barred by the amorphous layer, and can prevent generating of a spike of a cobalt silicide layer. And since the recrystallization is immersed by the cobalt silicide layer even if it extends a cobalt silicide layer to the depth in early stages of an amorphous layer and an amorphous layer recrystallizes in the case of the 2nd heat treatment, junction in the high recrystallization of resistance and a cobalt silicide layer is barred, and it can prevent that contact resistance goes up.